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| 1. | The resolution of an *n* bit DAC with a maximum input of 5 V is 5 mV. The value of *n* is |
| |  |  | | --- | --- | | [**A.**](javascript:%20void%200;) | 8 | | [**B.**](javascript:%20void%200;) | 9 | | [**C.**](javascript:%20void%200;) | 10 | | [**D.**](javascript:%20void%200;) | 11 |   **Answer:** Option **C**  **Explanation:**  https://www.indiabix.com/_files/images/electronics-and-communication-engineering/digital-electronics/69-418.png1000 = 5 or N = 10. |

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| 2. | 2's complement of binary number 0101 is |
| |  |  | | --- | --- | | [**A.**](javascript:%20void%200;) | 1011 | | [**B.**](javascript:%20void%200;) | 1111 | | [**C.**](javascript:%20void%200;) | 1101 | | [**D.**](javascript:%20void%200;) | 1110 |   **Answer:** Option **A**  **Explanation:**  1's complement of 0101 is 1010 and 2's complement is 1010+1 = 1011. |

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| 3. A device which converts BCD to seven segment is called |
| |  |  | | --- | --- | | [**A.**](javascript:%20void%200;) | encoder | | [**B.**](javascript:%20void%200;) | decoder | | [**C.**](javascript:%20void%200;) | multiplexer | | [**D.**](javascript:%20void%200;) | none of these |   **Answer:** Option **B**  **Explanation:**  Decoder converts binary/BCD to alphanumeric. |

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| 4. In 2's complement representation the number 11100101 represents the decimal number |
| |  |  | | --- | --- | | [**A.**](javascript:%20void%200;) | +37 | | [**B.**](javascript:%20void%200;) | -31 | | [**C.**](javascript:%20void%200;) | +27 | | [**D.**](javascript:%20void%200;) | -27 |   **Answer:** Option **D**  **Explanation:**  A = 11100101. Therefore A = 00011010 and A' = A + 1 = 00011011 = 16 + 8 + 2 + 1 = 27. Therefore A = -27. |

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| 5. A decade counter skips |
| |  |  | | --- | --- | | [**A.**](javascript:%20void%200;) | binary states 1000 to 1111 | | [**B.**](javascript:%20void%200;) | binary states 0000 to 0011 | | [**C.**](javascript:%20void%200;) | binary states 1010 to 1111 | | [**D.**](javascript:%20void%200;) | binary states 1111 to higher |   **Answer:** Option **C**  **Explanation:**  A decade counter counts from 0 to 9. It has 4 flip-flops. The states skipped are 10 to 15 or 1010 to 1111. |
| 6. BCD input 1000 is fed to a 7 segment display through a BCD to 7 segment decoder/driver. The segments which will lit up are |
| |  |  | | --- | --- | | [**A.**](javascript:%20void%200;) | *a, b, d* | | [**B.**](javascript:%20void%200;) | *a, b, c* | | [**C.**](javascript:%20void%200;) | all | | [**D.**](javascript:%20void%200;) | *a, b, g, c, d* |   **Answer:** Option **C**  **Explanation:**  1000 equals decimal 8 Therefore all segments will lit up.   |  |  | | --- | --- | | 7. A ring counter with 5 flip flops will have | | | |  |  | | --- | --- | | [**A.**](javascript:%20void%200;) | 5 states | | [**B.**](javascript:%20void%200;) | 10 states | | [**C.**](javascript:%20void%200;) | 32 states | | [**D.**](javascript:%20void%200;) | infinite states |   **Answer:** Option **A** | | |  | For the gate in the given figure the output will be https://www.indiabix.com/_files/images/electronics-and-communication-engineering/digital-electronics/33-457.png | | |  |  | | --- | --- | | [**A.**](javascript:%20void%200;) | 0 | | [**B.**](javascript:%20void%200;) | 1 | | [**C.**](javascript:%20void%200;) | A’ | | [**D.**](javascript:%20void%200;) | A |   **Answer:** Option **D**  **Explanation:**  If A = 0, Y = 1 and A = 1, Y = 0 Therefore Y = *A*. | | 8. In the expression A + BC, the total number of minterms will be | | | |  |  | | --- | --- | | [**A.**](javascript:%20void%200;) | 2 | | [**B.**](javascript:%20void%200;) | 3 | | [**C.**](javascript:%20void%200;) | 4 | | [**D.**](javascript:%20void%200;) | 5 |   **Answer:** Option **D** | |   A+BC = A (B+B') (C+C') + BC (A+A').  = (AB+AB') (C+C') + ABC + A'BC.  = ABC + ABC' + AB'C + AB'C' + ABC + A'BC.  = ABC + ABC' + AB'C + A'BC' + A'BC.   Since (ABC + ABC = ABC).   Hence 5 minterms.   |  | | --- | | 9. Which of the following is non-saturating? | | |  |  | | --- | --- | | **[A].** | TTL | | **[B].** | CMOS | | **[C].** | |  |  | | --- | --- | | ECL | @ | | | **[D].** | Both (a) and (b) |   **Answer:** Option **C** |   Emitter coupled logic (ECL) is a non saturated logic, which means that transistors are prevented from going into deep saturation, thus eliminating storage delays. Preventing the transistors from going into saturation is accomplished by using logic levels whose values are so close to each other that a transistor is not driven into saturation when its input switches from low to high. In other words, the transistor is switched on, but not completely on. This logic family is faster than TTL. Voltage level for high is -0.9 Volts and for low is -1.7V; thus biggest problem with ECL is a poor noise margin. |
| 10. The expression Y = M (0, 1, 3, 4) is |
| |  |  | | --- | --- | | [**A.**](javascript:%20void%200;) | POS | | [**B.**](javascript:%20void%200;) | SOP | | [**C.**](javascript:%20void%200;) | Hybrid | | [**D.**](javascript:%20void%200;) | none of the above |   **Answer:** Option **A**  **Explanation:**  This is product of sums expression.   |  |  | | --- | --- | |  | 11. Decimal 43 in hexadecimal and BCD number system is respectively. | | |  |  | | --- | --- | | [**A.**](javascript:%20void%200;) | B2, 01000011 | | [**B.**](javascript:%20void%200;) | 2B, 01000011 | | [**C.**](javascript:%20void%200;) | 2B, 00110100 | | [**D.**](javascript:%20void%200;) | B2, 01000100 |   **Answer:** Option **B**  **Explanation:**  (43)10 = (2B)16  (43)10 = (01000011)2 . |   Eg: 35710 = 0011 0101 0111 (BCD)   |  | | --- | | 12. The circuit of the given figure realizes the function https://www.indiabix.com/_files/images/electronics-and-communication-engineering/digital-electronics/30-397.png | | |  |  | | --- | --- | | [**A.**](javascript:%20void%200;) | Y = (A + B) C + DE | | [**B.**](javascript:%20void%200;) | Y = A + B + C + D + E | | [**C.**](javascript:%20void%200;) | AB + C +DE | | [**D.**](javascript:%20void%200;) | AB + C(D + E) |   **Answer:** Option **A**  **Explanation:**  https://www.indiabix.com/_files/images/electronics-and-communication-engineering/digital-electronics/68-397.png or  Y = (A + B)C + DE. | | 13. An AND gate has two inputs A and B and one inhibit input 3, Output is 1 if | | |  |  | | --- | --- | | [**A.**](javascript:%20void%200;) | A = 1, B = 1, S = 1 | | [**B.**](javascript:%20void%200;) | A = 1, B = 1, S = 0 | | [**C.**](javascript:%20void%200;) | A = 1, B = 0, S = 1 | | [**D.**](javascript:%20void%200;) | A = 1, B = 0, S = 0 |   **Answer:** Option **B**  **Explanation:**  All AND inputs must be 1 and inhibit 0 for output to be 1. | | 14. The greatest negative number which can be stored is 8 bit computer using 2's complement arithmetic is | | |  |  | | --- | --- | | **[A].** | - 256 | | **[B].** | |  |  | | --- | --- | | - 128 | @ | | | **[C].** | - 255 | | **[D].** | - 127 |   **Answer:** Option **B**  **Explanation:**  The largest negative number is 1000 0000 = -128.   |  |  | | --- | --- | |  | 15. A 12 bit ADC is used to convert analog voltage of 0 to 10 V into digital. The resolution is | | |  |  | | --- | --- | | [**A.**](javascript:%20void%200;) | 2.44 mV | | [**B.**](javascript:%20void%200;) | 24.4 mV | | [**C.**](javascript:%20void%200;) | 1.2 V | | [**D.**](javascript:%20void%200;) | none of the above |   **Answer:** Option **A**  **Explanation:**  https://www.indiabix.com/_files/images/electronics-and-communication-engineering/digital-electronics/69-408.png. | | 16. For the truth table of the given figure Y = https://www.indiabix.com/_files/images/electronics-and-communication-engineering/digital-electronics/29-384.png | | | |  |  | | --- | --- | | [**A.**](javascript:%20void%200;) | A + B + C | | [**B.**](javascript:%20void%200;) | A + BC | | [**C.**](javascript:%20void%200;) | A | | [**D.**](javascript:%20void%200;) | B |   **Answer:** Option **D**  **Explanation:**  Y = A B C + A B C + AB C + A B C = A B (C + C) + A B (C + C) = A B + AB = B(A + A) = B. | |  |  | | --- | | 17. A full adder can be made out of | | |  |  | | --- | --- | | [**A.**](javascript:%20void%200;) | two half adders | | [**B.**](javascript:%20void%200;) | two half adders and a OR gate | | [**C.**](javascript:%20void%200;) | two half adders and a NOT gate | | [**D.**](javascript:%20void%200;) | three half adders |   **Answer:** Option **B**  **Explanation:**  https://www.indiabix.com/_files/images/electronics-and-communication-engineering/digital-electronics/66-130.png | | |

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| 18. If the functions *w, x, y, z* are as follows. *w* = R + PQ + RS ,  *x* = PQR S + PQR S + PQ R S https://www.indiabix.com/_files/images/electronics-and-communication-engineering/digital-electronics/40-589-1.png https://www.indiabix.com/_files/images/electronics-and-communication-engineering/digital-electronics/40-589-2.png Then |
| |  |  | | --- | --- | | [**A.**](javascript:%20void%200;) | *w = z x = z* | | [**B.**](javascript:%20void%200;) | *w = z, x = y* | | [**C.**](javascript:%20void%200;) | *w = y* | | [**D.**](javascript:%20void%200;) | *w = y = z* |   **Answer:** Option **A**  **Explanation:**  Use k-map, then it will be easy |

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| 19. | Which device has one input and many outputs? |
| |  |  | | --- | --- | | [**A.**](javascript:%20void%200;) | Multiplexer | | [**B.**](javascript:%20void%200;) | Demultiplexer | | [**C.**](javascript:%20void%200;) | Counter | | [**D.**](javascript:%20void%200;) | Flip flop |   **Answer:** Option **B**  **Explanation:**  Demultiplexer takes data from one line and directs it to any of its N output depending on the status of its select lines. |

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| 20. A carry look ahead adder is frequently used for addition because |
| |  |  | | --- | --- | | [**A.**](javascript:%20void%200;) | it costs less | | [**B.**](javascript:%20void%200;) | it is faster | | [**C.**](javascript:%20void%200;) | it is more accurate | | [**D.**](javascript:%20void%200;) | is uses fewer gates |   **Answer:** Option **B**  **Explanation:**  In look ahead carry adder the carry is directly derived from the gates when original inputs are being added. Hence the addition is fast. This process requires more gates and is costly. |

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| 21. The counter in the given figure is https://www.indiabix.com/_files/images/electronics-and-communication-engineering/digital-electronics/35-483.png |
| |  |  | | --- | --- | | [**A.**](javascript:%20void%200;) | Mod 3 | | [**B.**](javascript:%20void%200;) | Mod 6 | | [**C.**](javascript:%20void%200;) | Mod 8 | | [**D.**](javascript:%20void%200;) | Mod 7 |   **Answer:** Option **B**  **Explanation:**  When counter is 110 the counter resets. Hence mod 6. |

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| 22.For the minterm designation Y = ∑ m (1, 3, 5, 7) the complete expression is |
| |  |  | | --- | --- | | [**A.**](javascript:%20void%200;) | Y = A BC + A B C | | [**B.**](javascript:%20void%200;) | Y = A B C + A B C + ABC + A BC | | [**C.**](javascript:%20void%200;) | Y = A B C + A B C + ABC + A BC | | [**D.**](javascript:%20void%200;) | Y = A B C + ABC + A BC + A BC |   **Answer:** Option **B**  **Explanation:**  Decimal number 1 = binary number 001 = A BC Decimal number 7 = binary number 111= ABC, Decimal number 3 = binary number 011= ABC Decimal number 5 = binary number 101= ABC . Hence result. |

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| Zero suppression is not used in actual practice. |
| |  |  | | --- | --- | | [**A.**](javascript:%20void%200;) | True | | [**B.**](javascript:%20void%200;) | False |   **Answer:** Option **B**  **Explanation:**  Zero suppression is commonly used |

**Zero suppression** is the removal of redundant zeroes from a number. This can be done for storage, page or display space constraints or formatting reasons, such as making a letter more legible.

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| 23. A counter type A/D converter contains a 4 bit binary ladder and a counter driven by a 2 MHz clock. Then conversion time |
| |  |  | | --- | --- | | [**A.**](javascript:%20void%200;) | 8 μ sec | | [**B.**](javascript:%20void%200;) | 10 μ sec | | [**C.**](javascript:%20void%200;) | 2 μ sec | | [**D.**](javascript:%20void%200;) | 5 μ sec |   **Answer:** Option **A**  **Explanation:**  https://www.indiabix.com/_files/images/electronics-and-communication-engineering/digital-electronics/70-564.png  The binary ladder is a resistive network whose output voltage is a properly weighted sum of the digital inputs. |
| 24. The number of distinct Boolean expression of 4 variables is |
| |  |  | | --- | --- | | [**A.**](javascript:%20void%200;) | 16 | | [**B.**](javascript:%20void%200;) | 256 | | [**C.**](javascript:%20void%200;) | 1024 | | [**D.**](javascript:%20void%200;) | 65536 |   **Answer:** Option **D**  **Explanation:**  22n = 224 = 216 . |

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| 25. A memory system of size 16 k bytes is to be designed using memory chips which have 12 address lines and 4 data lines each. The number of such chips required to design the memory system is |
| |  |  | | --- | --- | | [**A.**](javascript:%20void%200;) | 2 | | [**B.**](javascript:%20void%200;) | 4 | | [**C.**](javascript:%20void%200;) | 8 | | [**D.**](javascript:%20void%200;) | 18 |   **Answer:** Option **C**  **Explanation:**  **https://www.indiabix.com/_files/images/electronics-and-communication-engineering/digital-electronics/69-453.png (4096=2^12)**   |  | | --- | | 26. A three state switch has three outputs. These are | | |  |  | | --- | --- | | [**A.**](javascript:%20void%200;) | low, low and high | | [**B.**](javascript:%20void%200;) | low, high, high | | [**C.**](javascript:%20void%200;) | low. floating, low | | [**D.**](javascript:%20void%200;) | low, high, floating |   **Answer:** Option **D**  **Explanation:**  Third state is floating. |  |  | | --- | | 27. Maxterm designation for A + B + C is | | |  |  | | --- | --- | | [**A.**](javascript:%20void%200;) | M0 | | [**B.**](javascript:%20void%200;) | M1 | | [**C.**](javascript:%20void%200;) | M3 | | [**D.**](javascript:%20void%200;) | M4 |   **Answer:** Option **A**  **Explanation:**  A + B + C = 000 = M0 . |      |  | | --- | | **28. Assertion (A):** A demultiplexer can be used as a decoder.  **Reason (R):** A demultiplexer can be built by using AND gates only. | | |  |  | | --- | --- | | [**A.**](javascript:%20void%200;) | Both A and R are correct and R is correct explanation of A | | [**B.**](javascript:%20void%200;) | Both A and R are correct but R is not correct explanation of A | | [**C.**](javascript:%20void%200;) | A is true, R is false | | [**D.**](javascript:%20void%200;) | A is false, R is true |   **Answer:** Option **C**  **Explanation:**  Demultiplexer requires NOT gates also in addition to AND gates. |  |  | | --- | | 29. The number of bits in ASCII is | | |  |  | | --- | --- | | [**A.**](javascript:%20void%200;) | 12 | | [**B.**](javascript:%20void%200;) | 10 | | [**C.**](javascript:%20void%200;) | 9 | | [**D.**](javascript:%20void%200;) | 7 |   **Answer:** Option **D**  **Explanation:**  ASCII is a 7 bit code. | | 30. 4 bit 2's complement representation of a decimal number is 1000. The number is | | |  |  | | --- | --- | | [**A.**](javascript:%20void%200;) | + 8 | | [**B.**](javascript:%20void%200;) | 0 | | [**C.**](javascript:%20void%200;) | - 7 | | [**D.**](javascript:%20void%200;) | - 8 |   **Answer:** Option **D**  **Explanation:**  (a) and (d) both are option, But there is meaning to represent a positive number in 2's complement form, we take complement representation for negative number only. Therefore most appropriate number is "-8". | |  | |  | | 31. A 4 : 1 multiplexer requires \_\_\_\_\_\_\_\_\_\_ data select line. | | |  |  | | --- | --- | | [**A.**](javascript:%20void%200;) | 1 | | [**B.**](javascript:%20void%200;) | 2 | | [**C.**](javascript:%20void%200;) | 3 | | [**D.**](javascript:%20void%200;) | 4 |   **Answer:** Option **B**  **Explanation:**  22 = 4. Hence 2 select lines. |  |  | | --- | | 32. The number of unused states in a 4 bit Johnson counter is | | |  |  | | --- | --- | | [**A.**](javascript:%20void%200;) | 2 | | [**B.**](javascript:%20void%200;) | 4 | | [**C.**](javascript:%20void%200;) | 8 | | [**D.**](javascript:%20void%200;) | 12 |   **Answer:** Option **C**  **Explanation:**  Total state = 2*n* = 24 = 16  Used state = 2n = 2 x 4 = 8  Unused state = 16 - 8 = 8 | |
| 33. For a MOD-12 counter, the FF has a *tpd* = 60 ns The NAND gate has a *tpd* of 25 n sec. The clock frequency is |
| |  |  | | --- | --- | | [**A.**](javascript:%20void%200;) | 3.774 MHz | | [**B.**](javascript:%20void%200;) | 5.774 MHz | | [**C.**](javascript:%20void%200;) | < 3.774 MHz | | [**D.**](javascript:%20void%200;) | 4.167 MHz |   **Answer:** Option **A**  **Explanation:**  For a proper working, the clock period should be equal to or greater than  *tpd* = Mod 12 - 4FFs = 4 x 60 = 240 nsec.  Total *tpd* = 240 + 25 = 265 nsec.  = *fc*https://www.indiabix.com/_files/images/electronics-and-communication-engineering/digital-electronics/70-535.png and *fc* = 3.774 MHz. |

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|  | 34. An 8 bit data is to be entered into a parallel in register. The number of clock pulses required is |
| |  |  | | --- | --- | | [**A.**](javascript:%20void%200;) | 8 | | [**B.**](javascript:%20void%200;) | 4 | | [**C.**](javascript:%20void%200;) | 2 | | [**D.**](javascript:%20void%200;) | 1 |   **Answer:** Option **D**  **Explanation:**  In a parallel in register only one pulse is needed to enter data. |
| 35. Which of the following is error correcting code? | |
| |  |  | | --- | --- | | [**A.**](javascript:%20void%200;) | EBCDIC | | [**B.**](javascript:%20void%200;) | Gray | | [**C.**](javascript:%20void%200;) | Hamming | | [**D.**](javascript:%20void%200;) | ASCII |   **Answer:** Option **C**  **Explanation:**  Hamming code is widely used for error correction | |

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| 36. A universal shift register can shift |
| |  |  | | --- | --- | | [**A.**](javascript:%20void%200;) | from left to right | | [**B.**](javascript:%20void%200;) | from right to left | | [**C.**](javascript:%20void%200;) | both from left to right and right to left | | [**D.**](javascript:%20void%200;) | none of the above |   **Answer:** Option **C**  **Explanation:**  Both left to right and right to left operations are possible in universal shift register. |

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| 37. A16 X 216 \_\_\_\_\_\_\_\_\_\_ . |
| |  |  | | --- | --- | | [**A.**](javascript:%20void%200;) | 1616 | | [**B.**](javascript:%20void%200;) | 1516 | | [**C.**](javascript:%20void%200;) | 1416 | | [**D.**](javascript:%20void%200;) | 1316 |   **Answer:** Option **C**  **Explanation:**  A16 = 10, 216 = 2, 10 x 2 = 20 in decimal = 14 in hexadecimal. |

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| 38. The Boolean expression for the circuit of the given figure https://www.indiabix.com/_files/images/electronics-and-communication-engineering/digital-electronics/29-385.png |
| |  |  | | --- | --- | | [**A.**](javascript:%20void%200;) | A {F + (B + C) (D + E)} | | [**B.**](javascript:%20void%200;) | A [F + (B + C) (DE)] | | [**C.**](javascript:%20void%200;) | A + F + (B + C) (D + E)] | | [**D.**](javascript:%20void%200;) | A [F + (BC) (DE)] |   **Answer:** Option **A**  **Explanation:**  B and C in parallel give B + C. Similarly D and E in parallel give D + E. (B + C) in series with (D + E) give (B + C) (D + E). Since F is in parallel we get F + (B + C) (D + E). Finally A is in series. Therefore we get A[F + (B + C) (D + E)] |

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| 39. A counter has N flip flops. The total number of states are |
| |  |  | | --- | --- | | [**A.**](javascript:%20void%200;) | N | | [**B.**](javascript:%20void%200;) | 2 N | | [**C.**](javascript:%20void%200;) | 2N | | [**D.**](javascript:%20void%200;) | 4 N |   **Answer:** Option **C**  **Explanation:**  One flip-flop means 2 states and N flip-flops means 2N states. |

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| 40. A divide by 78 counter can be obtained by |
| |  |  | | --- | --- | | [**A.**](javascript:%20void%200;) | 6 numbers of mod-13 counters | | [**B.**](javascript:%20void%200;) | 13 numbers of mod-6 counters | | [**C.**](javascript:%20void%200;) | one mod-13 counter followed by mod-6 counter | | [**D.**](javascript:%20void%200;) | 13 number of mod-13 counters |   **Answer:** Option **C**  **Explanation:**  Modulus 13 x modulus 6 = modulus 78. |
| 41. The initial state of MOD-16 down counter is 0110. What state will it be after 37 clock pulses? |
| |  |  | | --- | --- | | [**A.**](javascript:%20void%200;) | Indeterminate | | [**B.**](javascript:%20void%200;) | 0110 | | [**C.**](javascript:%20void%200;) | 0101 | | [**D.**](javascript:%20void%200;) | 0001 |   **Answer:** Option **D**  **Explanation:**  A mod-16 counter goes through 16 states in one cycle of 16 Pulses.  It complete 2 cycles in 32 Pulses.  In the rest 5 Pulses, it moves down from 0110 = 610 - 510 = 110 or (001)2 . |

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| 42. The number of address lines in EPROM 4096 x 8 is |
| |  |  | | --- | --- | | [**A.**](javascript:%20void%200;) | 2 | | [**B.**](javascript:%20void%200;) | 4 | | [**C.**](javascript:%20void%200;) | 8 | | [**D.**](javascript:%20void%200;) | 12 |   **Answer:** Option **D**  **Explanation:**  212 = 4096. |

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|  | 43. In a mod-12 counter the input clock frequency is 10 kHz. The output frequency is |
| |  |  | | --- | --- | | [**A.**](javascript:%20void%200;) | 0.833 kHz | | [**B.**](javascript:%20void%200;) | 1.0 kHz | | [**C.**](javascript:%20void%200;) | 0.91 kHz | | [**D.**](javascript:%20void%200;) | 0.77 kHz |   **Answer:** Option **A**  **Explanation:**  Mod-12 counter is divide by 12 counter. Output frequency = https://www.indiabix.com/_files/images/electronics-and-communication-engineering/digital-electronics/69-471.png = 0.833 kHz. |
| 44. Quantization error occurs in | |
| |  |  | | --- | --- | | [**A.**](javascript:%20void%200;) | D/A converter | | [**B.**](javascript:%20void%200;) | A/D converter | | [**C.**](javascript:%20void%200;) | both D/A and A/D converter | | [**D.**](javascript:%20void%200;) | neither D/A nor A/D converter |   **Answer:** Option **B**  **Explanation:**  Analog input can have any value but digital value can have only 2N discrete levels (for N bits). Hence quantization error in A/D conversion. | |

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| 45. Which of these are universal gates? |
| |  |  | | --- | --- | | [**A.**](javascript:%20void%200;) | Only NOR | | [**B.**](javascript:%20void%200;) | Only NAND | | [**C.**](javascript:%20void%200;) | Both NOR and NAND | | [**D.**](javascript:%20void%200;) | NOR, NAND, OR |   **Answer:** Option **C**  **Explanation:**  Both NAND and NOR are called universal gates |

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| 46. Out of latch and flip flop, which has clock input? |
| |  |  | | --- | --- | | [**A.**](javascript:%20void%200;) | Latch only | | [**B.**](javascript:%20void%200;) | Flip flop only | | [**C.**](javascript:%20void%200;) | Both latch and flip flop | | [**D.**](javascript:%20void%200;) | None |   **Answer:** Option **B**  **Explanation:**  This the main difference between latch and flip-flop. Only flip-flop has clock input. |
| 47. In the given figure shows a 4 bit serial in parallel out right shift register. The initial contents as shown are 0110. After 3 clock pulses the contents will be https://www.indiabix.com/_files/images/electronics-and-communication-engineering/digital-electronics/32-443.png |
| |  |  | | --- | --- | | [**A.**](javascript:%20void%200;) | 0000 | | [**B.**](javascript:%20void%200;) | 0101 | | [**C.**](javascript:%20void%200;) | 1010 | | [**D.**](javascript:%20void%200;) | 1111 |   **Answer:** Option **C**  **Explanation:**  Output of XOR gate is input to register.   |  | | --- | | 48. On the fifth clock pulse, a 4-bit Johnson sequence is Q0 = 0, Q1 = 1, Q2 = 1, and Q3 = 1. On the sixth clock pulse, the sequence is \_\_\_\_\_\_\_\_. | | |  |  | | --- | --- | | [**A.**](javascript:%20void%200;) | Q0 = 1, Q1 = 0, Q2 = 0, Q3 = 0 | | [**B.**](javascript:%20void%200;) | Q0 = 1, Q1 = 1, Q2 = 1, Q3 = 0 | | [**C.**](javascript:%20void%200;) | Q0 = 0, Q1 = 0, Q2 = 1, Q3 = 1 | | [**D.**](javascript:%20void%200;) | Q0 = 0, Q1 = 0, Q2 = 0, Q3 = 1 |   **Answer:** Option **C** | |
| 49.  \_\_\_\_\_\_ logic is mostly used in microprocessor chips. a. TTL b. DTL c. CMOS d. NMOS  Answer: C |
| 50. The minimum number of NAND gates required to perform EX-NOR gate is a. 3 b. 4 c. 5 d. 6  Answer: C  51. The minimum number of NOR gates required to perform EX-OR gate is a. 4 b. 5 c. 6 d. 3  Answer: A  52. The EX-OR gate is also called a. Inequality circuit b. 1 bit comparator c. Difference circuit d. All of the above  Answer: D |

 53. The forbidden input condition is present in  
a. RS flip-flop  
b. D flip-flop  
c. JK flip-flop  
d. T flip-flop

Answer: A

54. When both J and K inputs of edge triggered JK flip-flop are ‘1’, then the flip-flop is in  
a. Race condition  
b. Synchronous condition  
c. Asynchronous condition  
d. Toggle condition

Answer: D

55. Generally \_\_\_\_\_\_\_\_\_\_ flip-flops are used in shift registers.  
a. D  
b. T  
c. SR  
d. JK

Answer: D

56. A counter in which the output of one flip-flop acts as clock for other is termed as  
a. Synchronous counter  
b. Ripple counter  
c. Ring counter  
d. Decoder

Answer: A

57. The minimum number of flip-flops required for a MOD-14 counter is  
a. 7  
b. 4  
c. 5  
d. 14

Answer: B

58. Counters are used in measurement of  
a. Frequency  
b. Time  
c. Distance  
d. All of the above

Answer: A

Which of the following counter results in least delay  
a. Ring counter  
b. Ripple counter  
c. Synchronous counter  
d. Asynchronous counter

Answer: B